Multi-core Processor Considerations in Modern Day SoC Designs

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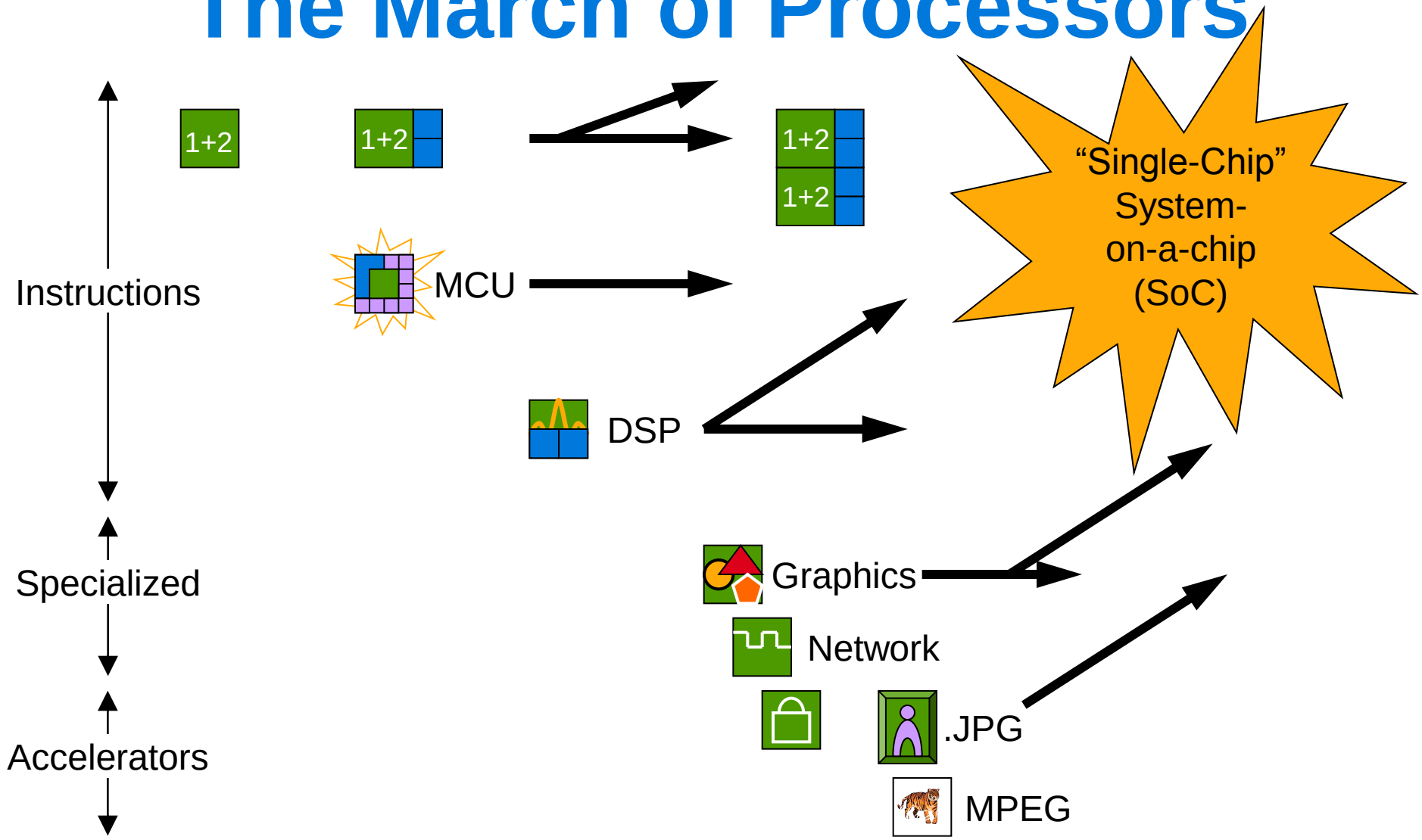
OBJECTIVE ANALYSIS
SEMICONDUCTOR MARKET RESEARCH

Strategy Sanity

The March of Processors



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Three Steps to Processor Use

- Select the Processors
- Build the Processor Complex
- Program the Processors

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A Balance of Processors Perform the Required Tasks

- General-Purpose Processor
- DSP
- Specialty Processors
- Accelerators

- Task Partitioning
- Architecture (ARM, MIPS, PowerPC…)
- Performance (MHz…)
- Flexibility
- Coordination

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Assemble Processors into the SoC

- Memory Hierarchy
- Bus Structure
- Voltage, Clock, and Power Domains
- Process Technology
- SoC and SiP
- EDA / Development Tool Integration
- Validation
- Verification
- Simulation
- Emulation

- Power Dynamics

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Application Programs Make the SoC Functional

- Operating System
- Application Programs
- User Interface
- Off-the-shelf

- APIs
- CODECs
- IP Stacks
- Interfaces

- Partitioned to Selected Processors
- Integrated
- Conflict-free
- Tested, Certified

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Multi-Processor SoC

Current Examples

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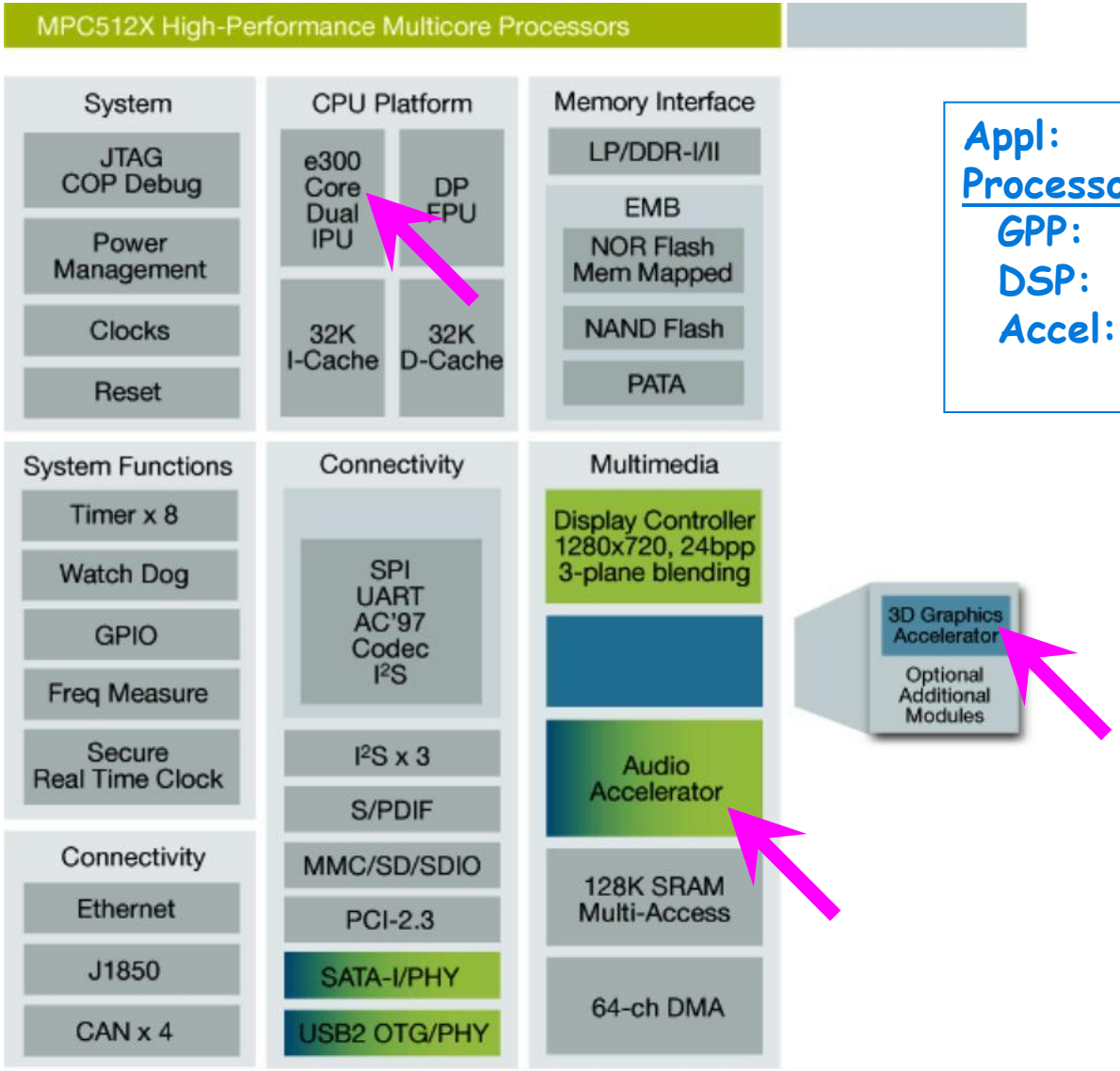
Freescale



Appl: General
Processors:
GPP: PowerPC e300 w/ Float
DSP: <none>
Accel: 3D Graphics
Audio

source: Freescale Semiconductors

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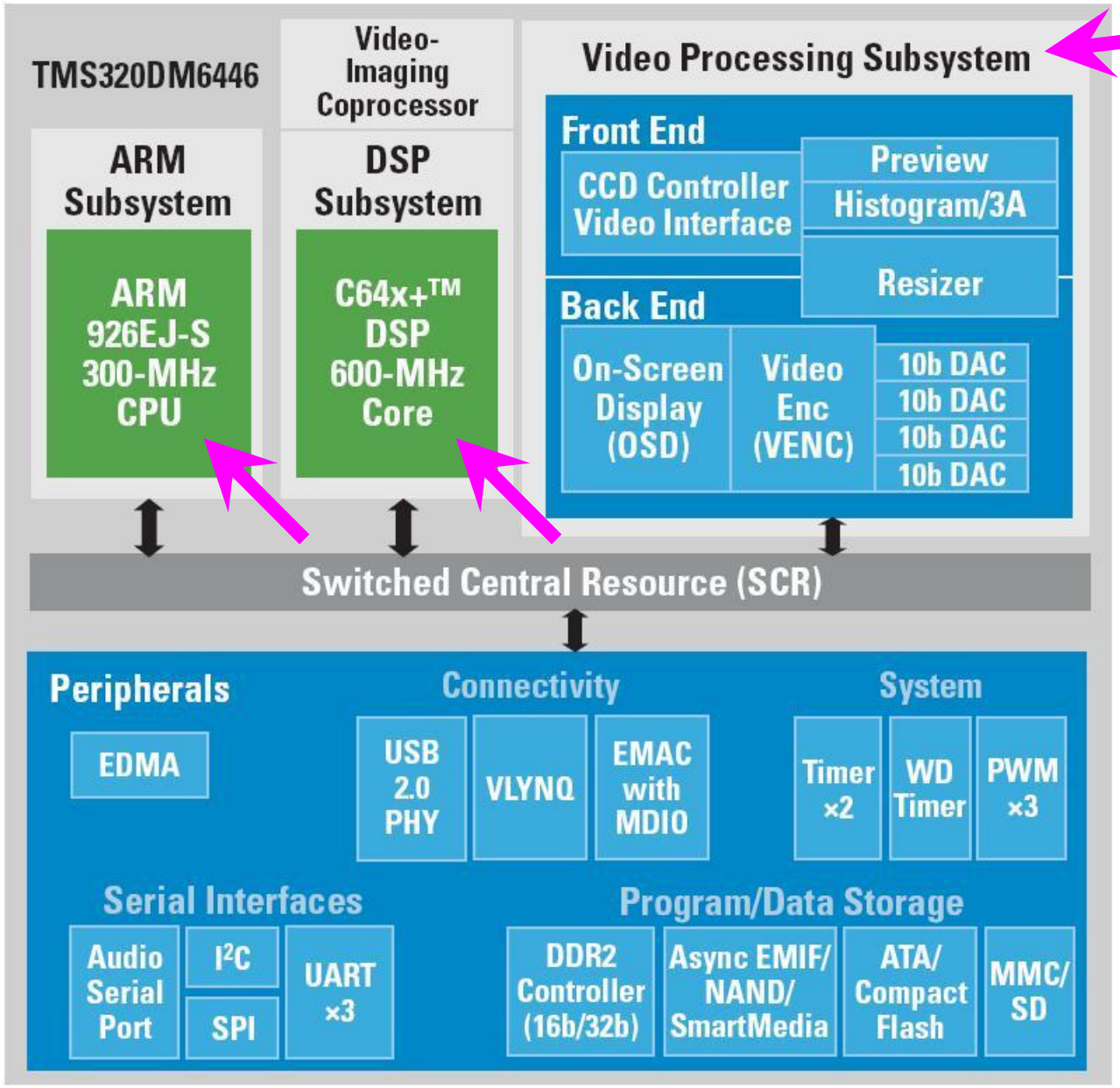
Texas Instruments – DaVinci



Appl: Video-oriented

Processors:

GPP: ARM 926EJ-S

DSP: TI 320C64x

Accel: Video/Imaging

ARM-specific memory:

16KB Instruction Cache
16KB Data Cache
16KB RAM
16KB ROM

DSP-specific memory:

32KB Instruction RAM/Cache
80KB Data RAM/Cache
64KB Level 2 RAM/Cache

source: Texas Instruments

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Texas Instruments – OMAP Evolution

Appl: Handsets, PDA

OMAP Model	331	750	16xx 17xx	2420	2430	3410	3420 3430	VOX 2230	eCosto 1035
General-Purpose Processor	ARM 926	ARM 926E-J	ARM 926E-J			ARM Cortex A8	ARM Cortex A8	ARM 926E-J	ARM 926E-J
		ARM 7		ARM 1136	ARM 1136			ARM 1136	
DSP		C54x	C55x	C55x				C55x	C55x
Image A							ISP		
Video A				IVA	IVA 2	IVA 2	IVA 2	IVA 2	
Graphics		2D	2D	3D	3D	-	PowerVR	3D	2D
Digital RF									DRP

source: Texas Instruments

A = Accelerator
ISP = Image Signal Processor
IVA = Image Video & Audio A
2D/3D = 2-/3-dimensional graphics A
DRP = Digital Radio Processor

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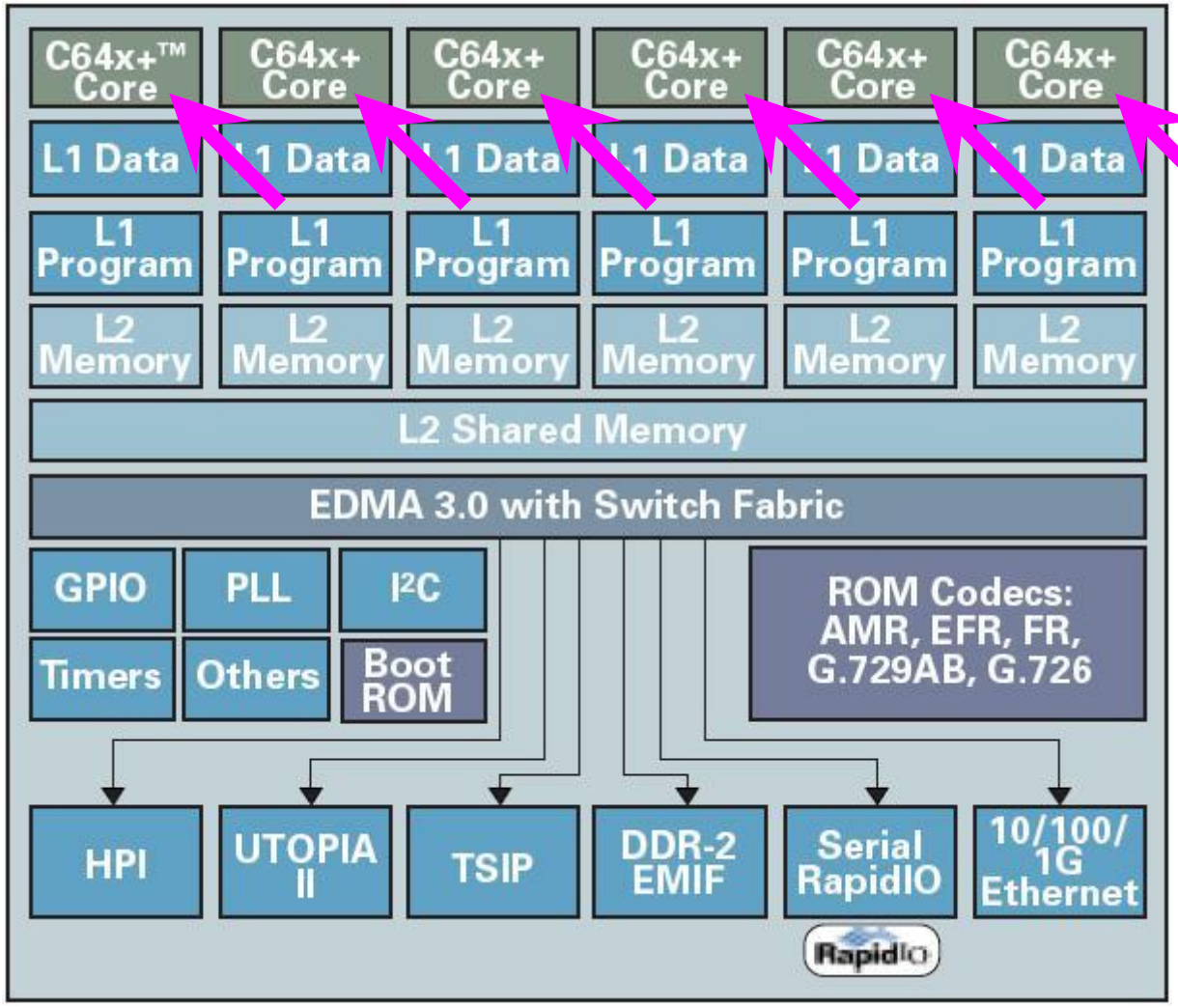
Texas Instruments – Ultra DSP



Appl: Communication Infrastructure

Processors:

GPP: <none>

DSP: 6: TI 320C64x

Accel: <none>

DSP-specific memory: (6 each)

32KB Instruction RAM/Cache
32KB Data RAM/Cache
96KB Level 2 RAM/Cache

source: Texas Instruments

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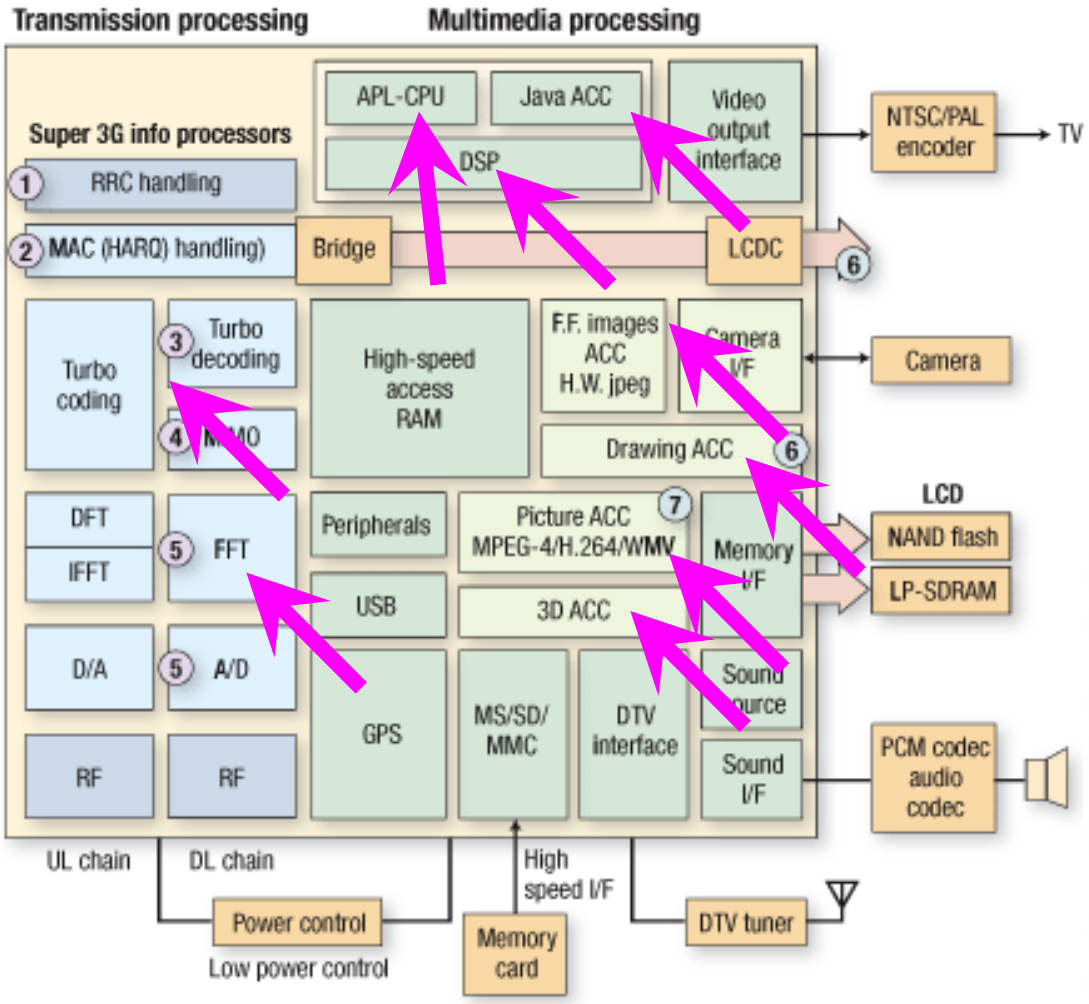
Docomo – Future Phone

Docomo maps out ideal long-term evolution processor

Integrated chip would power cell phones with data rates of as much as 100 Mbits/s



1. Simplification
2. Increasing loads by shortening TTI (example: 2ms-1ms)
3. High-speed turbo processing, parallel processing
4. Double receiving function circuit scale with the implementation of MIMO
5. High-speed FFT processing (example: FFT max, 2,048, sampling rate 30.72 Mbits/s)
6. High-definition-capable
7. High-definition multi-compatible codec

source: NTT Docomo as presented in EETimes

Appl: Cellular handset

Processors:

- **GPP:** one
- **DSP:** one
- **Accel:** Many

anity

Multiple Processors Are Here

Deal With It !

- Sophisticated Issues
- Balance to the System Needs
- Critical to Execution:
  - Integrated End-to-End Tools
  - Software, Software, Software

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Definitions

MPU = Microprocessor

MCU = Microcontroller

DSP = Digital Signal Processor

RAM = Random Access Memory

MHz = Megahertz (clock frequency)

ARM = Popular processor architecture available as intellectual property (IP) from Advanced RISC Machines, ARM Ltd

MIPS = Popular processor architecture available as IP from MIPS Technology Inc.

PowerPC = Popular processor architecture managed by IBM and Freescale, with limited availability in IP form

SoC = system-on-a-chip

SiP = system-in-a-package (multi-chip, stacked…)

JPG ~ JPEG = Joint Picture Experts Group

MPEG = Motion Picture Experts Group

API = Application Program Interface

CODEC = coder/decoder

IP = intellectual property

IP = Internet Protocol

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