Multicore 101:
The Architectural Options

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EE Times Virtual Conference: Approaching Multicore

Tom Starnes
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Tom Starnes is an industry analyst following many aspects of the embedded processor industry. Mr. Starnes started his career neck-deep in embedded microprocessors explaining and marketing these new products for Motorola (now Freescale) for over 15 years back when the 68000 ruled the marketplace. He has spent the last 15 years as an industry analyst watching, encouraging, and advising the vendors, strategies, products, and applications of all forms of embedded processors, from microcontrollers to digital signal processors (DSP) and high performance processor cores. A frequent writer, reference, speaker, instructor and sounding board, Mr. Starnes is well known in the industry for his realistic views of the needs and direction of processors in embedded applications. He now runs Strategy Sanity, consulting one-on-one with clients including the financial community regarding semiconductor companies, products, markets, and outlooks. He also performs traditional market research working with Objective Analysis (www.objective-analysis.com) and other independent firms.

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Panelists

Bob Doud
Director of Processor Strategy, Tilera

Bill Graham
Product Marketing Manager,
VxWorks, Wind River

Markus Levy
Founder and President, EEMBC

Steve Jahnke
Chief Architect, Linux Systems,
Wireless Business Unit, Texas Instruments

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Bob Doud
Director of Processor Strategy, Tilera
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Bob brings more than 25 years experience in the networking, silicon and security industries to Tilera. He has previously worked at a number of networking silicon companies including Hifn, NetOctave and SafeNet in roles ranging from Sr. System Architect to Product Line Director. Bob also spent a number of years in the security appliance industry in both engineering and lead technologist roles, giving him a strong background in the design requirements and challenges in bringing hardware & software systems to market. Bob received a Bachelor's degree, cum laude, in Physics and Math from Ohio Wesleyan University.
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Bill Graham
Product Marketing Manager,
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Bill Graham is the product marketing manager for VxWorks platforms at Wind River. He has over 20 years of experience in the software industry, including embedded and real-time systems development, UML modeling, and object-oriented design. Prior to joining Wind River, Bill held marketing and product management positions at QNX, IBM Rational, and Klocwork. Prior to his career in marketing, Bill was a software engineer at ObjecTime, Cross Keys and Lockheed Martin. Bill holds a Bachelor's and Master's Degree in Electrical Engineering from Carleton University in Ottawa, Canada.

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Markus Levy
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Markus Levy is founder and president of EEMBC. He is also president of The Multicore Association and chairman of two technical conferences, the Multicore Expo and the ARM Developers' Conference. Mr. Levy was previously a senior analyst at In-Stat/MDR and an editor at EDN magazine, focusing in both roles on processors for the embedded industry. Levy began his career in the semiconductor industry at Intel Corporation, where he served as both a senior applications engineer and customer training specialist for Intel's microprocessor and flash memory products. He is the co-author of Designing with Flash Memory, the one and only technical book on this subject, and received several patents while at Intel for his ideas related to flash memory architecture and usage as a disk drive alternative.

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Steve Jahnke
Chief Architect, Linux Systems,
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As the Linux chief architect for the Texas Instruments Incorporated (TI) wireless business unit, Steve Jahnke drives the overall Linux software architecture on TI's OMAP(tm) platform. In this role, Jahnke ensures that the OMAP silicon features are fully entitled in all Linux-based devices, in all stages of development - from architecture and design, to testing and final release. During his close to 15 years at TI, Jahnke has held several roles focused on System-on-Chip (SoC) and software design for the automotive, communication and consumer electronic markets. He earned a master's degree in electrical engineering from Rice University, and a bachelor's degree in electrical engineering from Northwestern University.

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Single Processors Worked Beautifully

- Single processors have been just fine until a couple years ago
- All applications benefit from simple frequency increases
- Superscalar & multi-threading implementations improved efficiency without significant re-coding of programs – the chip or compiler did the work

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Moore's Law Hits Speed Bump

- Static power consumption overcomes Dynamic power as high-speed semiconductor process nodes approach 65nm
- Could not continue simply increasing clock speed
- Power consumption creates heat that must be dissipated
  - Heat sink, airflow, fan, air conditioning, enclosures, reliability

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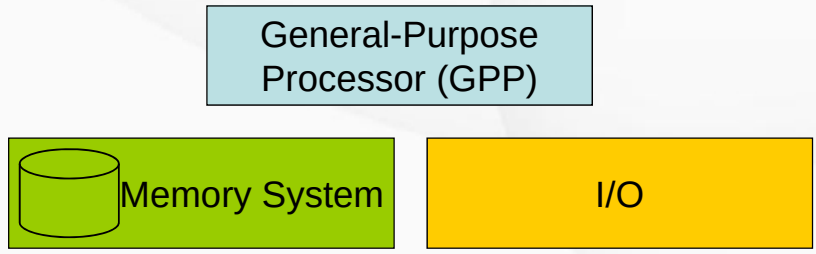
Divide and Conquer – Multi-Core

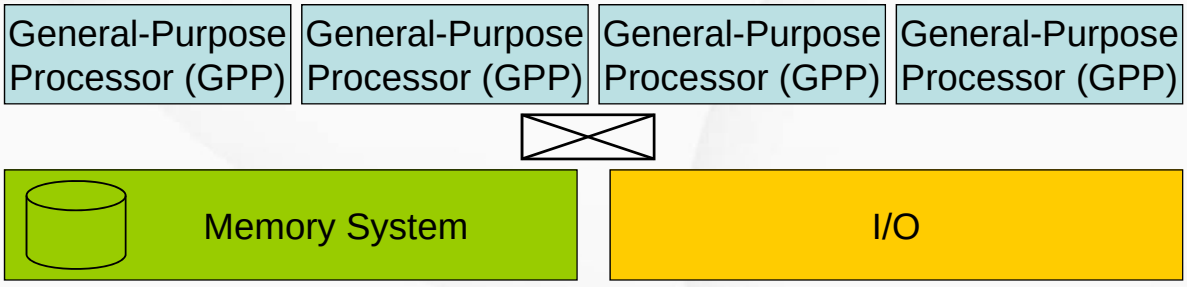
- Replicate processor cores to multiply performance but stay within the frequency range of a reasonable power envelope
- The hardware is fairly easy
  - But memory (cache) must be managed
  - But program sequences must be managed
- Oh, but the software may not divide up so well!
  - On the other hand, this could be a special advantage to some applications

Multi-Core Styles

- Homogenous
  - Symmetric Multi-Processing (SMP)
  - Asymmetric Multi-Processing (AMP)
  - Many-Core
- Heterogeneous



Homogeneous Multi-Core



- Familiar general-purpose processors, sharing memory & I/O resources – one chip savings
  - Can be DSPs… too

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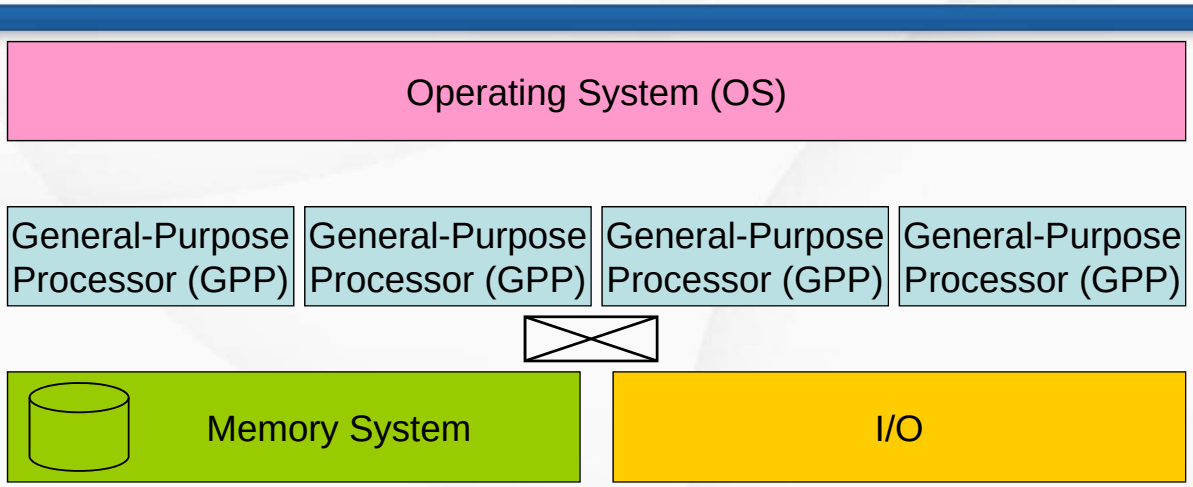
Symmetric MultiProcessing (SMP)



- Operating System distributes and manages load across all processors and resources
  - Delays from coordination, set-up, and bottlenecks

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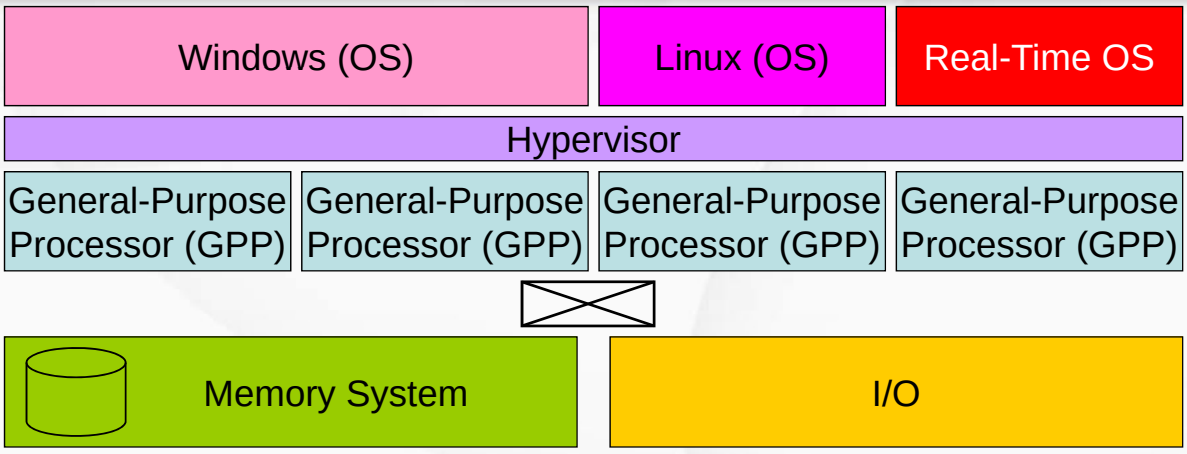
Asymmetric MultiProcessing (AMP)



➔ Processor cores assigned to specific OS's

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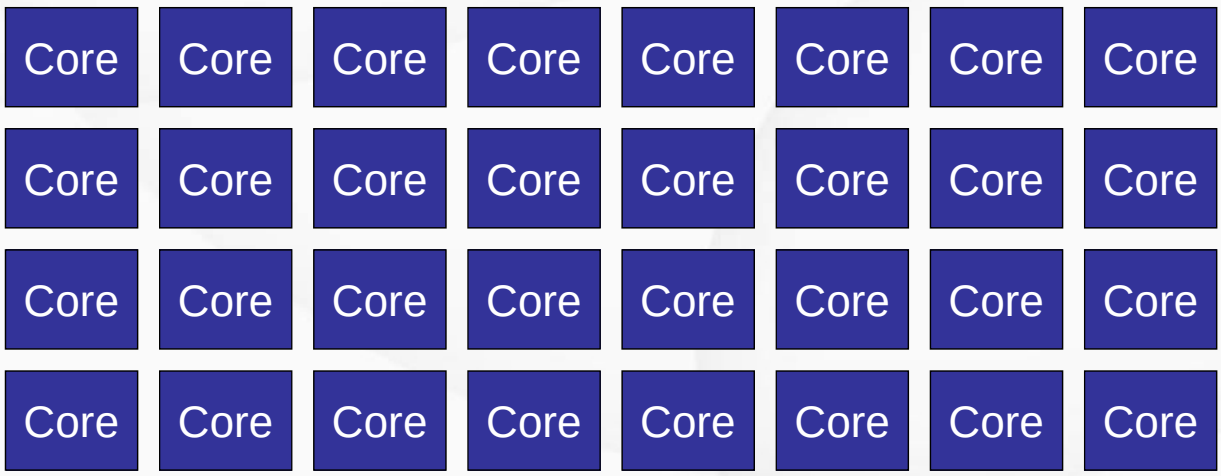
Many-Core



➔ Same processor attacks same problem
– en masse

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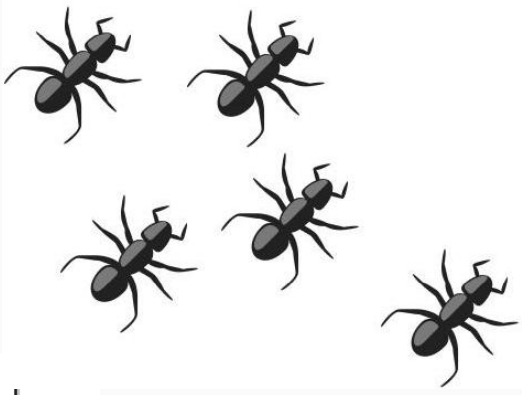
It's The Natural Way



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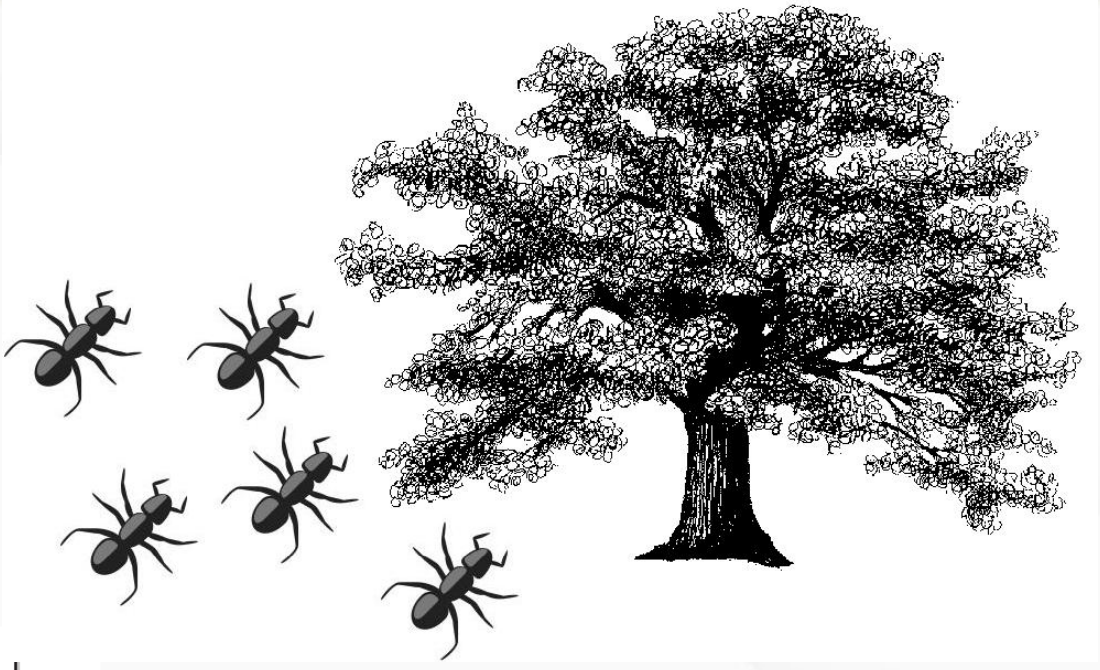

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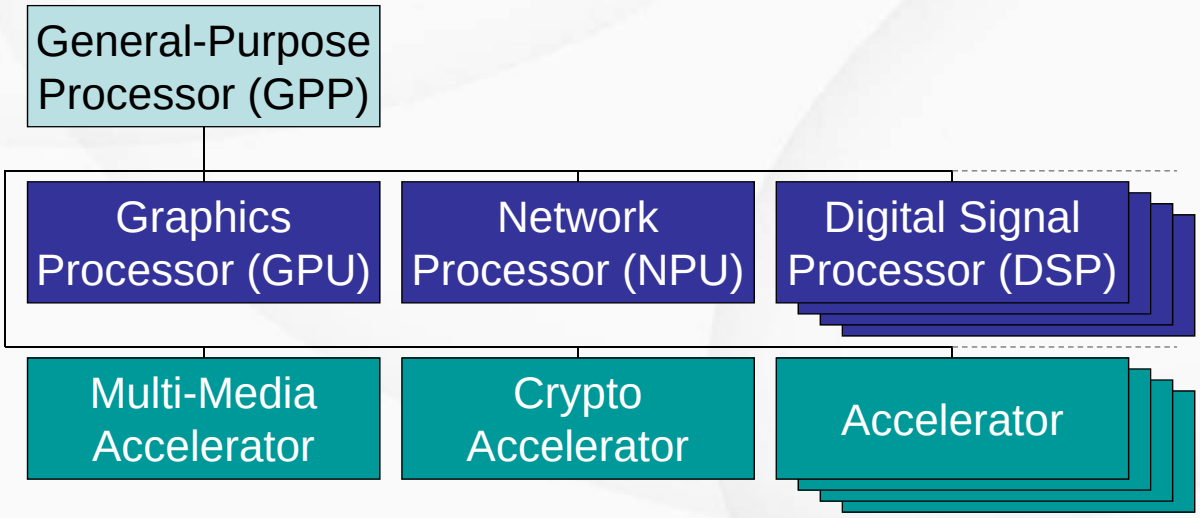
Heterogeneous Multi-Core



➔ Specialization gains big in efficiency (power)

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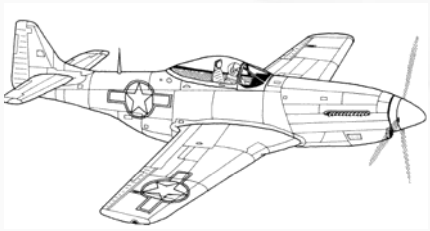
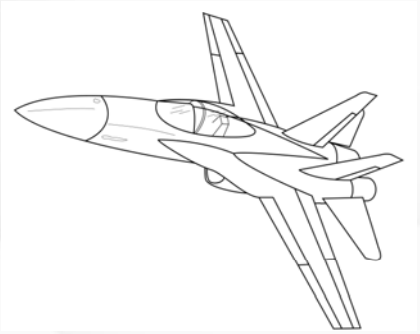
Approaching Multi-Core

- Beyond a GigaHertz
- Processor Paradigm Shift
- Multi-Core is Inevitable
- "Deal with it!"





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Question – SMP, AMP, Many, Het

- How does a person determine the Multi-Core organization to use for their application?
  - Homogeneous
  - Symmetric Multiprocessing (SMP)
  - Asymmetric Multiprocessing (AMP)
  - Many-Core
  - Heterogeneous

Question – What Parallelizes

- What are the characteristics of applications that lend themselves well to parallelization?
- What applications parallelize well? Is Multi-Core just for PC/servers, HPC, and network infrastructure?
- How does the use of multiple Operating Systems make Multi-Core particularly attractive?

Question – Non-parallelizable

- For applications that do not parallelize well, what do they do when they hit the speed bump (run out of single-core gas)?
- When is it best to use heterogeneous processors? What are the downsides?

Question – Characterize

- Characterize the jump to Multi-Core. What kind of project do I compare it to?
  - Brand New Product Development
  - Complete Redesign
  - Product Extension
  - New Feature
  - Huge Undertaking
    - "Special Team"
  - Iterate, Iterate, Iterate
  - Feed Through a Tool
  - No Sweat

Is it better to make going to Multi-Core a parallel effort or replace normal upgrade cycle?

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Question – Change ISA

- Is the jump to Multi-Core significant enough to consider changing the Instruction Set Architecture (ISA)?

Question – Steps

- How does the system designer of a single-stream application approach Multi-Core? What steps should be taken to determine the best approach for the specific application?

Question – Multi-Core Pluses

- From the application side, what are the fundamental advantages to multiple cores? Negatives?

Question – Always Multi-Core

- If it can be done on single core, are there situations where Multi-Core should still be attempted? Why?

Question – Software or Hard

- Is Multi-Core largely a software issue rather than a hardware issue to system designers?

Questions from Conference Attendees

- Please submit your questions for our panelists now.

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