Software Development Tools for Multicore Systems

Brought to you by:

Tom Starnes
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Tom Starnes is an industry analyst following many aspects of the embedded processor industry. Mr. Starnes started his career neck-deep in embedded microprocessors explaining and marketing these new products for Motorola (now Freescale) for over 15 years back when the 68000 ruled the marketplace. He has spent the last 15 years as an industry analyst watching, encouraging, and advising the vendors, strategies, products, and applications of all forms of embedded processors, from microcontrollers to digital signal processors (DSP) and high performance processor cores. A frequent writer, reference, speaker, instructor and sounding board, Mr. Starnes is well known in the industry for his realistic views of the needs and direction of processors in embedded applications. He now runs Strategy Sanity, consulting one-on-one with clients including the financial community regarding semiconductor companies, products, markets, and outlooks. He also performs traditional market research working with Objective Analysis (www.objective-analysis.com) and other independent firms.

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EE Times Virtual Conference:
Approaching Multicore

Panelists

Martin Bakal,
Worldwide Market Manager,
Electronics Industry, IBM Rational

Tasneem Brutch,
Senior Staff Engineer, Samsung Electronics

Skip Hovsmith,
Director Applications Engineering, Critical Blue

Rob Oshana,
Distinguished Member of Technical Staff and Director of Global Software Research and Development for the Networking and Multimedia group, Freescale Semiconductor

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Martin Bakal is a worldwide market manager at IBM. He has a BS in electrical engineering and a master of science degree in engineering management, both from Tufts University. Bakal has consulted on numerous embedded projects from the Lockheed Martin on the Joint Strike Fighter (JSF) project to working with various customers in the automotive industry. Previously, he worked at Phar Lap Software (a Real-Time Operating System vendor) as a Technical Support Manager.

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Tasneem Brutch is a Senior Staff Engineer at Samsung Research, in San Jose, CA. She holds a B.S. in Computer Science and Engineering, a Masters in Computer Science, and a Ph.D. in Computer Engineering from Texas A&M University. She has approximately 13 years of industry experience, working as Sr. Engineer at Hewlett-Packard and as an Architect at Intel. At HP, she worked on the Host-Based Intrusion Detection System, in the Enterprise Systems Technology Lab. In addition to internal multicore and parallel computing research, Tasneem is Samsung Electronics' representative to the Multicore Association (MCA), Khronos Group, and Embedded Microprocessor Benchmarking Consortium (EEMBC) standards organizations' Board of Directors.

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Skip Hovsmith is the director of application engineering in the US for CriticalBlue, working on accelerating embedded software for multi-core systems, including parallel multi-core programming, legacy code migration, and coprocessor synthesis for software acceleration. Prior to CriticalBlue, Skip worked for several start ups in formal verification, FPGA design, and enterprise software services, and at National Semiconductor working on virtual prototyping, hw/sw co-design, reconfigurable systems, and standard cell product design. Skip received his BS in electrical engineering and computer science from Princeton University with a focus in engineering physics, and he holds several patents.

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Rob Oshana has over 28 years of experience in the real-time embedded industry in both applications as well as tools technology development. He is currently Distinguished Member of Technical Staff and Director of Global Software Research and Development for the Networking and Multimedia group at Freescale Semiconductor. He is widely published in the industry and speaks regularly at industry events. Rob has chaired international standards committees in the embedded space and is a licensed professional engineer. He is also an adjunct lecturer at Southern Methodist University and the University of Texas.

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Tools Get Tougher

- Everything you love and hate about Development Tools on single-core processors: Ditto on Multi-Cores, but more-so
- All the types of cores must be well-supported
- Caches, crossbars, I/O, IRQ, Modeling and simulation as complex as chip
- More hiding on-chip to observe, track, debug
- More tools must play nicely together
- Only as good as weakest link

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Programmer Must Think Differently

- Multi-Core practice is a fairly new field
- Sea-change of thinking about software
  Sequential ➔ Parallel
- Determinism gets worse – or better
- Tools always lag hardware
- Tools influence time-to-market, quality
- With the coming of age of Multi-Core, professional help now available

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Multi-Core in a Nutshell

➔ Jon & Kate plus Eight

➔ Octo-Mom

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Question – Ecosystem Status

- What is the state of development tools for Multi-Core systems?
  - What is in good shape?
  - What has room to improve?
- What tools are more critical in Multi-Core that weren't in single?

Question – It Takes More

- What is at the root of the difficulty of programming for Multi-Core?
  - Determining on which core to launch a process?
  - Constraints through memory?
  - Coherency?
  - Inter-core communications?
  - Basic resource allocation?
  - Are the operating systems (OS) adequate?
- Do we just need the mass volumes applied to working out better solutions?

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Question – Been There

- Multi-processing at the board- or system-level isn't new. Why is single-chip, Multi-Core processing any different?
- Shouldn't off-the-shelf Multi-Core chips help by minimizing options with a handful of fixed platforms?

Question – Tools Standards

- Tell us about the Development Tools Infrastructure Working Group and some standards you hope to establish?
- Is it Multi-Core-specific?
- How will heterogeneous cores complicate tool standards and interchange?
- Will vendors buy into it?

Question – Parallelize

- How do I break out sections of code to run in parallel? What granularity do I seek? How accurately can I predict final results?

Question – Gain / Core

- What performance gain can I expect from each additional core?
- Are there categories we can pin down?
- Diminishing returns or all you can eat?
- How will development tools improve my results?

Question – Chip or 3rd Party

- How good are the silicon vendors tools for Multi-Core processors?
- What advantage do independent 3rd-party development tools bring?
- What is needed to encourage better tool development?
- Is the business model right?
- Where is the expertise?

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Question – ISA Support

- What drives an independent tool vendor to support an instruction set architecture (ISA)?
- Does this become more involved when we move to multiple cores?
- Will the tool vendors need to narrow their focus?
- What sort of techniques might work on one ISA but not another?
- Will Multi-Core lock the application tighter to the ISA?

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Questions from Conference Attendees

- Please submit your questions for our panelists now.

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Thank You for Attending:

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